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Xyce™ Parallel Electronic Simulator Release Notes

Release 2.0

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Scope/Product Definition

The **Xyce** Parallel Electronic Simulator has been written to support, in a rigorous manner, the simulation needs of the Sandia National Laboratories electrical designers. Specific requirements include, among others, the ability to solve extremely large circuit problems by supporting large-scale parallel computing platforms, improved numerical performance and object-oriented code design and implementation.

The **Xyce** release notes describe:

- Hardware and software requirements
- New features and enhancements
- Any defects fixed since the last release
- Current known defects and defect workarounds

For up-to-date information not available at the time these notes were produced, please visit the **Xyce** web page at http://www.cs.sandia.gov/xyce.

Hardware/Software

This section gives basic information on supported platforms and hardware and software requirements for running **Xyce** 2.0.

Supported Platforms

Xyce 2.0 currently supports any of the following operating system (all versions imply the earliest supported – **Xyce** generally works on later versions as well) platforms. These platforms are supported in the sense that they have been subject to certification testing for the **Xyce** version 2.0 release.

- SGI IRIX® 6.5.21, Workshop Compilers 7.4.1 (serial and parallel using SGI MPI 4.3) Note: SGI IRIX® and Workshop Compilers are currently unstable. As of this release, most of the Sandia SGI machines are in the process of being upgraded. This process has not gone smoothly, and the situation will not stabilize until January 2004. Therefore, to run **Xyce** 2.0 on the Sandia SGI machines may require new builds.
- Redhat Linux®, version 8.0 on Intel Pentium® architectures (serial and parallel using MPICH or LAM MPI)
- Tru64 on HP/Compaq Alpha® (serial and parallel)
- FreeBSD on Intel Pentium® architectures (serial and parallel using MPICH or LAM MPI)
- Microsoft Windows® (serial)
- Apple® OS X (serial)

Build Capability but Not Supported

The platforms listed in this section are ”not supported” in the sense that they are not subject to nightly regression testing, and they also were not subject to certification testing for the **Xyce** version 2.0 release. For large parallel platforms, such as ASCI White, this sort of testing is not a realistic option. These platforms are supported in the sense that **Xyce** 2.0 has been built for these platforms, and successfully executed on them. If a user needs to run **Xyce** 2.0 on one of these platforms, contact the **Xyce** team and we will work with you on a case-by-case basis.

- Sun Microsystems Solaris 8.0, on UltraSPARC and later architectures (serial)

- CPlant™ on HP/Compaq Alpha® (serial)
- ASCI White (IBM) (parallel)

Hardware Requirements

The following are estimated hardware requirements for running **Xyce**:

- 128MB memory recommended, 64 MB memory minimum – *memory requirements increase with circuit size*
- 200MB disk space

Software Requirements

Several libraries (all freely available from Sandia National Laboratories and other sites) are required to build **Xyce** on a platform. These are only required when building **Xyce** from source. These are:

- Trilinos Solver Library (Sandia, http://software.sandia.gov/Trilinos) . This is a suite of libraries including Amesos, AztecOO, Epetra, EpetraExt, Ifpack, NOX, LOCA, and y12m.
- SuperLU (http://www.nersc.org)
- Xyce Expression library (libexpr.a).
- BLAS (libblas.a).
- LAPack (liblapack.a).

For parallel builds, the following are additionally required:

- MPI (http://www-unix.mcs.anl.gov/mpi/) library for message passing (version 1.1 or higher), such as MPICH or LAM
- Zoltan (Sandia, http://www.cs.sandia.gov/Zoltan) and its associated libraries (libzoltan.a, libzoltanCPP.a, libparmetis.a, libmetis.a)
- Chaco (Sandia, http://www.cs.sandia.gov/CRF/chaco) (libchaco.a, libChacoCPP.a (Xyce-version))

Xyce Release 2.0 Documentation

The following **Xyce** documentation is available at the **Xyce** internal website in pdf form. Some of this documentation is in Draft mode and is incomplete.

- **Xyce** Users' Guide, Version 2.0
- **Xyce** Reference Guide, Version 2.0
- **Xyce** Release Notes, Version 2.0
- **Xyce** Theory Document
- **Xyce** Test Plan

New Features and Enhancements

This release is the first full release following the Version 1.1 release. It encompasses many key bug fixes as well as key robustness and performance enhancements. Furthermore, many features that we previously provided as options have now been thoroughly tested and are now defaults (e.g., direct-matrix access for improved performance). Lastly, several new features continue to move **Xyce** towards a more full-featured circuit simulation tool. Highlights for this release are listed below. For details of each of these options statements, see the **Xyce** Users' Guide, and the **Xyce** Reference Guide.

- Improved parser performance.
- More extensive support for PDE devices.
- Stability enhancements to the prompt photocurrent models.
- The NOX nonlinear solver as the default nonlinear solver.
- Support for homotopy algorithms with NOX/LOCA. In particular, these algorithms are very useful for solving large MOSFET circuits.
- New support for .STEP analysis.
- Improved compatibility with other circuit simulators (PSpice, ChileSPICE).

Device Support

Devices supported in **Xyce**2.0 are the same as for the previous release (1.1). A number of the devices have been revised to improve robustness. The complete device list is given in the table below:

Device	Comments
Capacitor	Age-aware, semiconductor
Inductor	Nonlinear mutual inductor (see below)
Nonlinear Mutual Inductor	Sandia Core model (not fully PSpice compatible)
Resistor	Semiconductor
Diode (Level 1)	
Diode (Level 3)	Prompt photocurrent radiation model
Independent Voltage Source (VSRC)	
Independent Current Source (ISRC)	
Voltage Controlled Voltage Source (VCVS)	
Voltage Controlled Current Source (VCCS)	
Current Controlled Voltage Source (CCVS)	
Voltage Controlled Current Source (CCCS)	
Nonlinear Dependent Source (B Source)	
Bipolar Junction Transistor (BJT)(Level 1)	
Bipolar Junction Transistor (BJT)(Level 3)	Prompt photocurrent radiation model.
MOSFET (Level 1)	
MOSFET (Level 3)	
MOSFET (Level 9)	BSIM3 model.
Transmission Line	Lossless.
Voltage Controlled Switch (VSWITCH)	
PDE Devices (Level 1)	one-dimensional
PDE Devices (Level 2)	two-dimensional

Table 1: Devices Supported by Xyce.

Robustness Improvements

- The addition of homotopy algorithms has led to **Xyce** being much more robust for large MOSFET circuits.
- The radiation models (Diode and BJT) have been made less susceptible to roundoff

error, and now support breakpoints for discontinuity capturing.

Interface Improvements

- The netlist parser has been optimized. The optimization came about due to improvements in the handling of device metadata.

Miscellaneous

- E, F, G, and H dependent voltage sources are now PSpice compatible.
- PSpice “M” parameter for simulation of parallel mosfets in ASIC modeling now supported.

Defects Fixed in this Release

Defect	Description
Non-existant nodes in .PRINT statement ignored. [Bug 40]	Requesting printing of a non-existant node now generates a warning.
Mixed alphanumeric node names mishandled in expressions. [Bug 157]	This has been fixed, and the restrictions on node names used in expressions are no longer necessary.
Photocurrent devices missing breakpoints. [Bug 167]	These devices (BJT level 2, diode level 2) now set integration breakpoints at all discontinuities of the pulsed radiation source.
Small circuits were causing parallel runs of **Xyce** to fail. [Bug 291]	Improved parallel support for small circuits. **Xyce** can more robustly handle small circuits in parallel, although there are still some limitations.
Checkpoint files from the initial transient time would not correctly restart a simulation. [Bug 330]	This is now fixed, and will work as expected.
TABLE expressions mishandled if extraneous spaces present. [Bug 332]	This has been fixed, and superfluous whitespace in the TABLE expression is now ignored.
Initial condition parsing problem under obscure conditions. [Bug 335]	This bug has been fixed and capacitor initial conditions now work irrespective of their context.
Model statements contained within subcircuits that had model parameters defined in terms of subcircuit parameters would not be defined correctly in all subcircuit instances. [Bug 353]	This is now fixed, and will work as expected.

Defect	Description
Incorrect parsing of capacitors with both model name and capacitance value. [Bug 374]	This has been fixed, and Xyce now recognizes this style of capacitance specification per the Reference Guide.
Garbage output when V(Voltage source name) requested [Bug 382]	This is now caught and recognized as a fatal error. Only nodal voltages may be output.
Segfault when invalid model type encountered. [Bug 387]	Invalid model types now cause Xyce exit cleanly with an appropriate error message.
Segfault when invalid device instance encountered. [Bug 401]	Device lines for unrecognized device (as might occur if a textual comment were somehow accidentally uncommented) types now cause fatal error message.

Table 2: Fixed Defects.

Known Defects and Workarounds

Defect	Description
`.DC` sweep output.	`.DC` sweep calculation does not automatically output sweep results. *Workaround:* Use `.PRINT` statement to output sweep variable results.
Failure for netlists using ChileSPICE digital primitives.	**Xyce** does not currently support the use of digital primitives. This will be available in the next release.
Xyce will not accept string parameters as models.	*Workaround:* Use integer for these values instead.
Failures for parallel runs of small circuits.	This problem is usually encountered for relatively small circuits ($<$10 devices), which should generally be run in serial. *Workaround:* Run problem in serial version of **Xyce**.
Subcircuit instances can have their default parameters improperly overridden and no longer accessible.	*Workaround:* Specify at least one parameter on the subcircuit instance line for any subcircuit defined with a parameter list.
Functions defined with `.FUNC` must use all parameters given in the declaration	*Workaround* Make sure that function definition uses all parameters that appear in the function declaration.
Using an invalid continuation option in the `.OPTIONS LOCA` block causes a core dump	*Workaround* Use only values of 0, 1 or 2 for the `.OPTIONS LOCA CONTINUATION=<parameter>` option.

Table 3: Known Defects and Workarounds.

Incompatibilities With Other Circuit Simulators

Issue	Comment
.SAVE does not work.	**Xyce** does not support this. Use .PRINT instead.
.OP is not complete	A .OP netlist will run in **Xyce**, but will not produce the extra output normally associated with the .OP statement.
Pulsed source rise time of zero.	A requested pulsed source rise/fall time of zero really is zero in Xyce. In other simulators, requesting a zero rise/fall time causes them to use the printing interval found on the .TRAN line.
Mutual Inductor Model.	Not the same as PSpice. This is a Sandia developed model but is compatible with Cadence PSpice parameter set.
.PRINT line shorthand.	Output variables have to be specified as V(node) or I(source). Specifying the node alone will not work.
BSIM3 level.	In **Xyce** the BSIM3 level=9. Other simulators have different levels for the BSIM3.
Node names vs. device names.	Currently, circuit nodes and devices MUST have different names in **Xyce**. Some simulators can handle a device and a node with the same name, but **Xyce** cannot.
Interactive mode.	**Xyce** does not have an interactive mode.
ChileSPICE-specific ”operating point voltage sources.”	These are not currently supported within **Xyce**. *However...* **Xyce** does support ”IC=<value>” statements for capacitors and inductors which will automatically set these voltage drops at the beginning of a transient simulation.
Syntax for .STEP is different.	See the Users’ Guide for details. The differences will be corrected in a later release.
Meaning of **Tstart** on .TRAN line different.	Most simulators use the **Tstart** parameter as the time to begin saving output. **Xyce** uses it simply as an offset applied to the time variable. To get behavior identical to that of PSpice or ChileSPICE with a nonzero **Tstart**, use a zero **Tstart** in **Xyce**, and discard output prior to the desired time using a .OPTIONS OUTPUT command.

Table 4: Incompatibilities with other circuit simulators.

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Trademarks

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